

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Kaoru NARITA

Appln. No. 09/421,273

Filed: October 20, 1999



Group Art Unit: 2825

Examiner: Unknown

For: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the document which is listed on the attached Form PTO-1449 and/or listed herein and which the Examiner may deem relevant to patentability of the claims of the above-identified application.

1. Steven H. Voldman et al., "Shallow Trench Isolation Double-Diode Electrostatic Discharge Circuit and Interaction with Dram Output Circuitry", EOS/ESD SYMPOSIUM, pp. 5B.7.1-5B.7.12.

One copy of the listed document is submitted herewith.

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A. Jenuro

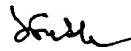
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TECHNICAL INFORMATION

Kaoru NARITA
Q56320
INFORMATION DISCLOSURE STATEMENT

The present Information Disclosure Statement is being filed (1) no later than three months from the application's filing date or (2) before the mailing date of the first Office Action on the merits (whichever is later), and therefore no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

The submission of the listed document is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



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